M37640E8/M8 8-bit MCU
12Mbps USB

This slide presentation includes:

- *Attractive Features for USB System design*
- *Distinctive Features*
- *Pin Configuration*
- *Block Diagram*
- *Enabling Quick System Development*
- *Others (Processor Modes, DMA Features…)*

MITSUBISHI 8-Bit Single-chip Microcomputer
740 Family / 764x Group

M37640 Attractive Features for USB System Design

- A high speed 5 endpoints USB function controller supports all USB transfer types: Isochronous, Bulk, Control and Interrupt.

- Operates in both self-powered and bus-powered applications; also, remains powered during USB suspend mode using <200uA.

- Isochronous Data Rate (via EP1):
  IN [(512 Bytes in FIFO)/2] x 1000frames/sec x 8 = 2Mbps
  OUT [(800 Bytes out FIFO)/2] x 1000frames/sec x 8 = 3.2Mbps

- Bulk Data Rate (via EP1): can support the theoretical maximum transfer rate of 19 64-byte packets/frame.

- The built-in DC-to-DC converter eliminates the need of an external 3.3V power supply (converts from 4.15V~5.25V to 3.3V).

- The built-in analog transceiver (USB V1.1 Spec.) eliminates the need for an external device.

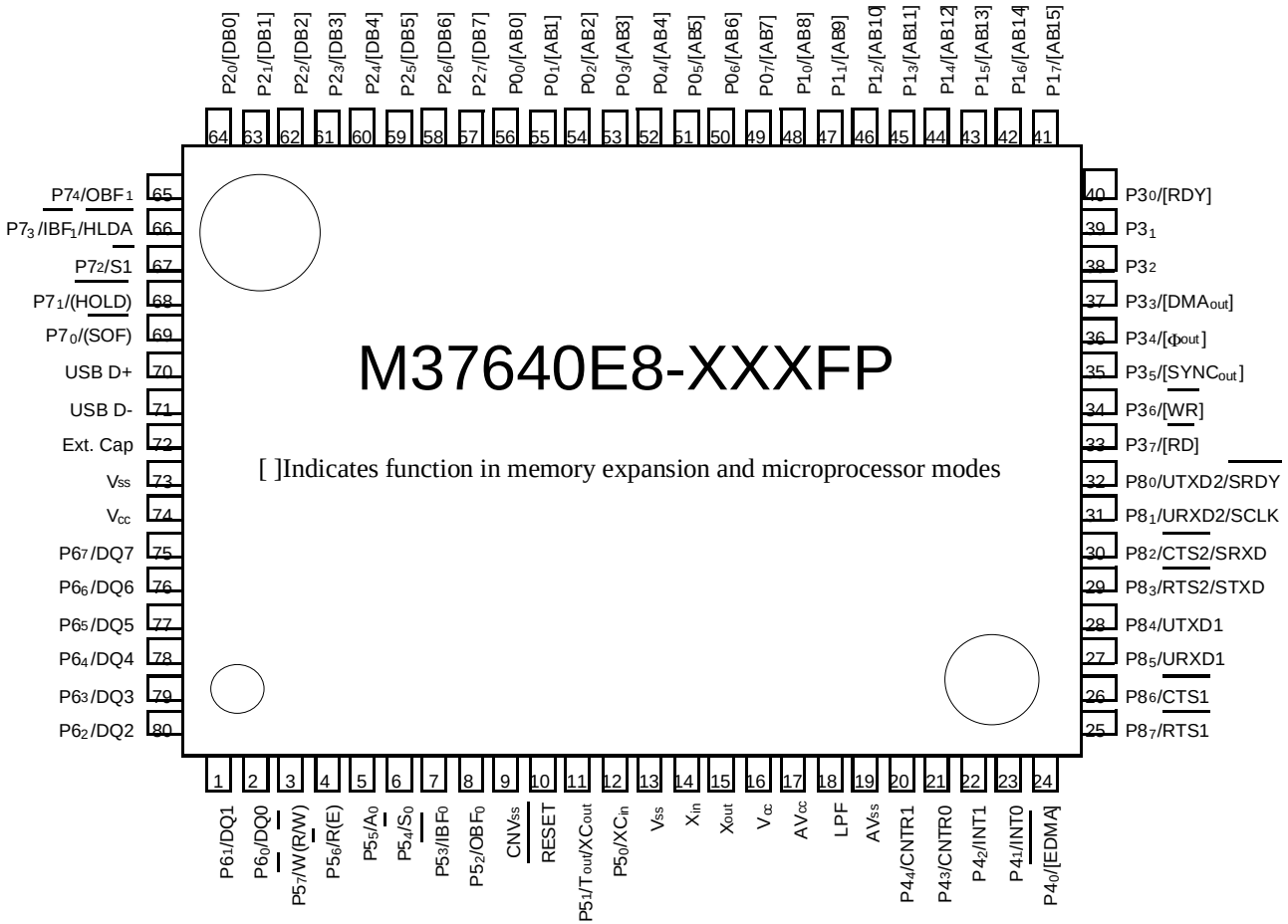
M37640 Attractive Features for USB System Design (con't)

- An internal PLL provides the 48 MHz clock for the USB block . This eliminates the need for an external 48mhz clock source and helps reduce overall system EMI.
- Two independent DMA channels provide an efficient means of transferring USB data between the USB FIFOs and other peripherals.
- The Intel 8042-compatible bus interface enables the M37640 to operate in a master/slave mode and to communicate with an external Host (or master) CPU at transfer rates up to ~3Mbytes; the Master is then free, while M37640 handles the local tasks.
- 8 Key-on Wake-up pins provide a way of returning from a STOP or WAIT mode by the touch of a key pad.
- Two different external clock inputs (Xin<24MHz and Xcin<5MHz) can be used for low-power operation mode or for keeping real time.
- A programmable special count source generator can be used to create various frequencies: fout=fin x[m/(m+1)]x[(1/(n+1)].

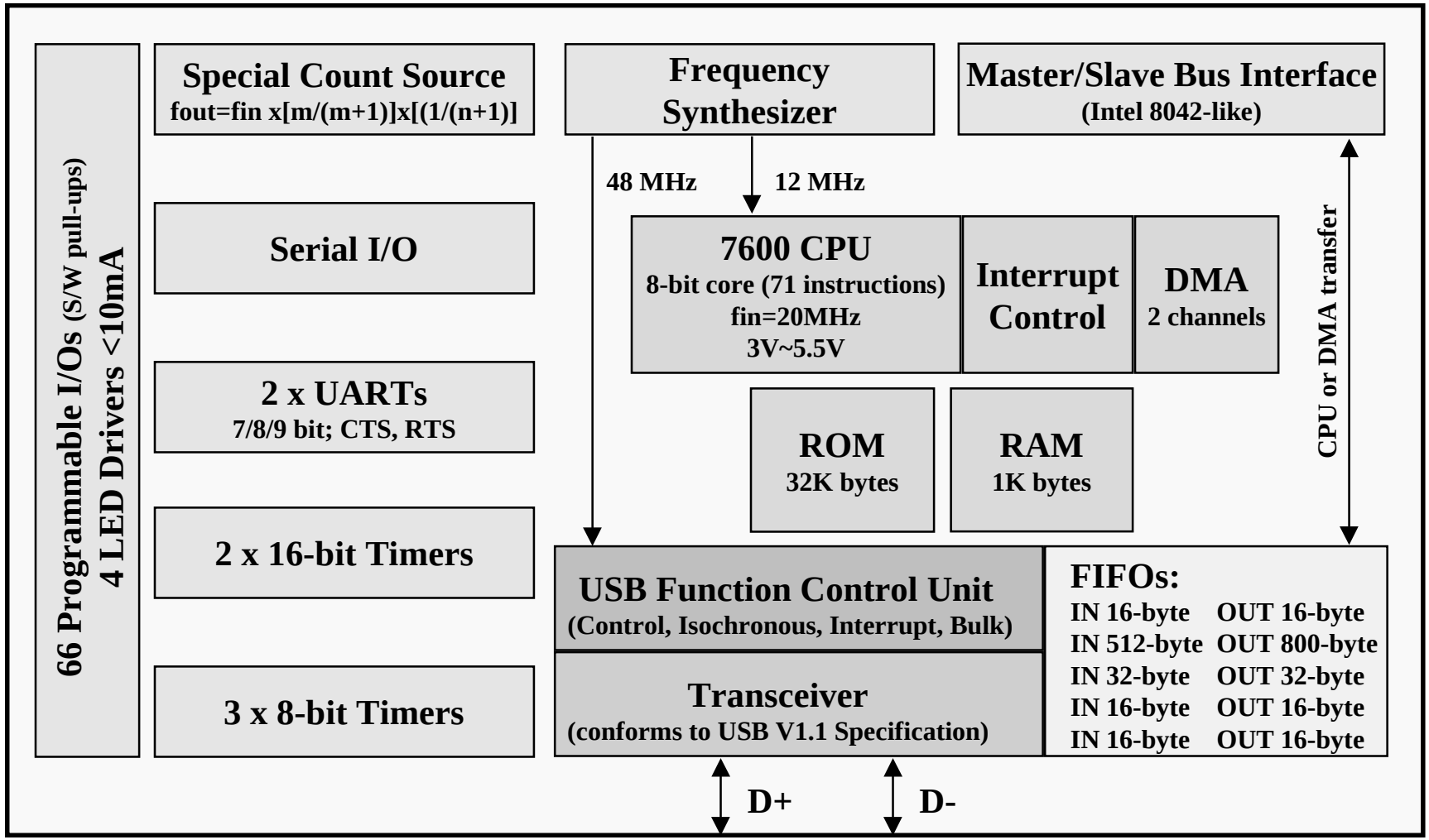
M37640 Distinctive Features

PARAMETERS			FUNCTION DESCRIPTION
Number of basic instructions			71
Instruction execution time (minimum)			83ns at Φ = 12 MHz (setting Φ to less than 5MHz is NOT recommended)
Clock frequency (maximum)			Xin = 48 MHz, XCin = 5 MHz (square wave), Φ= 12 MHz
Clock multiplier option			External clock Xin and XCin can be selectively divided and multiplied by X to create system internal clock Φ
Memory size	ROM		32K bytes
	RAM		1K bytes
Input / Output ports	P0~P3, P5, P6, P8	I/O	8-bit X 7 (Port 2 has a key-on wake-up feature)
	P4, P7	I/O	5-bit X 2
USB Function Control			FIFO: Endpoint 0: IN 16-byte, OUT 16-byte Endpoint 1: IN 512-byte, OUT 800-byte Endpoint 2: IN 32-byte, OUT 32-byte Endpoint 3: IN 16-byte, OUT 16-byte Endpoint 4: IN 16-byte, OUT 16-byte
Master CPU bus interface			DQ(7:0), $\overline{R}$(E), $\overline{W}$(R/$\overline{W}$), $\overline{S_0}$, $\overline{S_1}$, A_0, $\overline{IBF_0}$, OBF_0, $\overline{IBF_1}$, OBF_1; total of 17 signals interface with master CPU (Intel 8042-like interface)
Special Count Source Generator(SCSG)			Baud rate synthesizer
UART X 2			7/8/9-bit character length, with $\overline{CTS}$, $\overline{RTS}$ available
Serial I/O			8-bit clock synchronous serial I/O, supports both master and slave modes
Timers			8-bit X 3, 16-bit X 2
DMAC			2 channels, 16 address lines, support single byte or burst transfer modes
Software selectable slew rate control			Ports P0 ~ P8
Interrupts			4 external, 19 internal, 1 software, 1 system interrupts
Supply voltage			Vcc = 4.15 ~ 5.25V
External memory expansion			Memory Expansion and Microprocessor mode
External Data Memory Access (EDMA)			Allows > 64 K byte data access for instruction LDA (indY) and STA (indY)
Device structure			CMOS
Package			80P6N
Operating temperature range			-20 to 85◦C

M37640 Pin Configuration



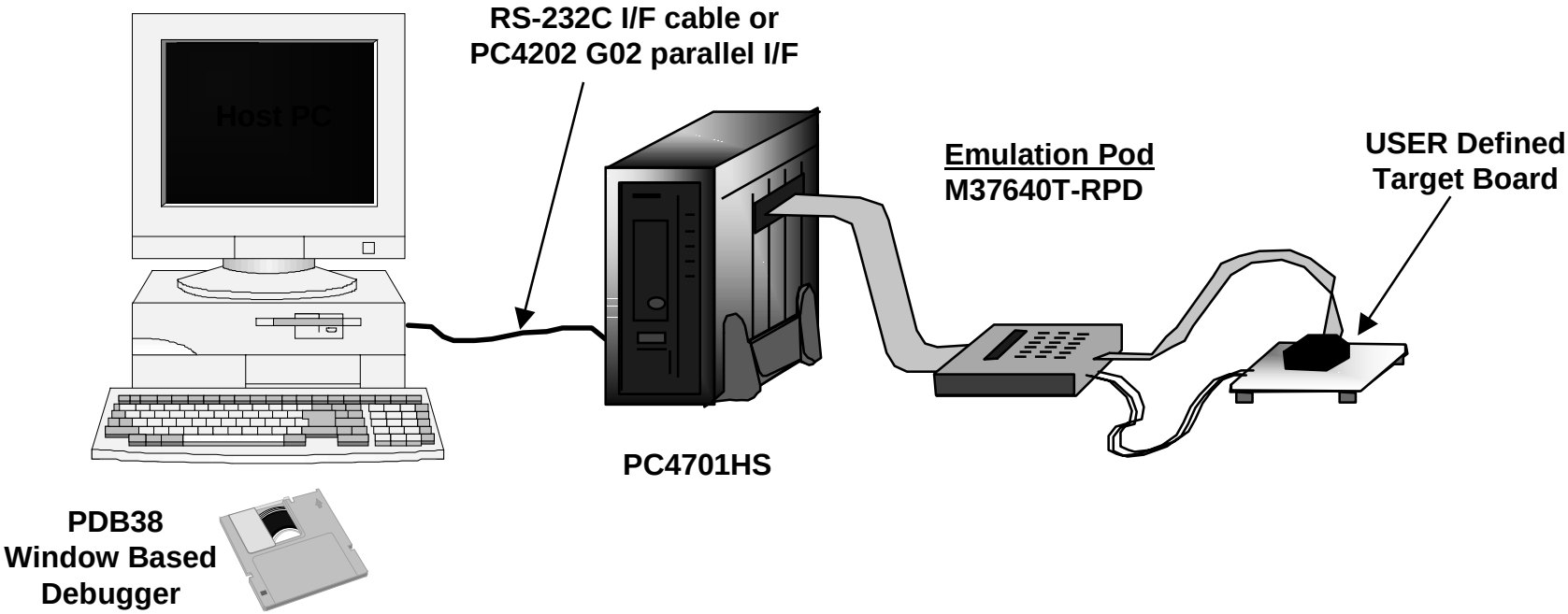
M37640 USB MCU Block Diagram



data sheets available: www.mitsubishichips.com/data/datasheets/mcus/m3769x/m3769x.htm

Enabling Quick System Development

- Various Sample Programs:
  - USB Enumeration Code
  - Peripheral Initialization S/W Routines
- Various Application Notes/Diagrams
- Erasable EPROM and OTP Devices
- Programming adapter
- In Circuit Emulator



Processor Modes

Single Chip Mode

- All internal memory is accessible
- All dedicated pins behave as I/O ports

Memory Expansion Mode

- All internal memory is accessible
- External memory (up to 64K minus internal memory) can be accessed as well
- Four 8-bit ports become Address, Data and Control signals
- Slow memory wait and EDMA can be enabled

M37640 Additional Features

- Slow Memory Wait
  When interfacing with external memory that is too slow to operate at the normal read/write speed of the MCU, a wait can be used to extend the read/write cycle.

- Hold Function
  The hold function is used when the MCU is part of a system where more than one device will need control of the external address and data buses.

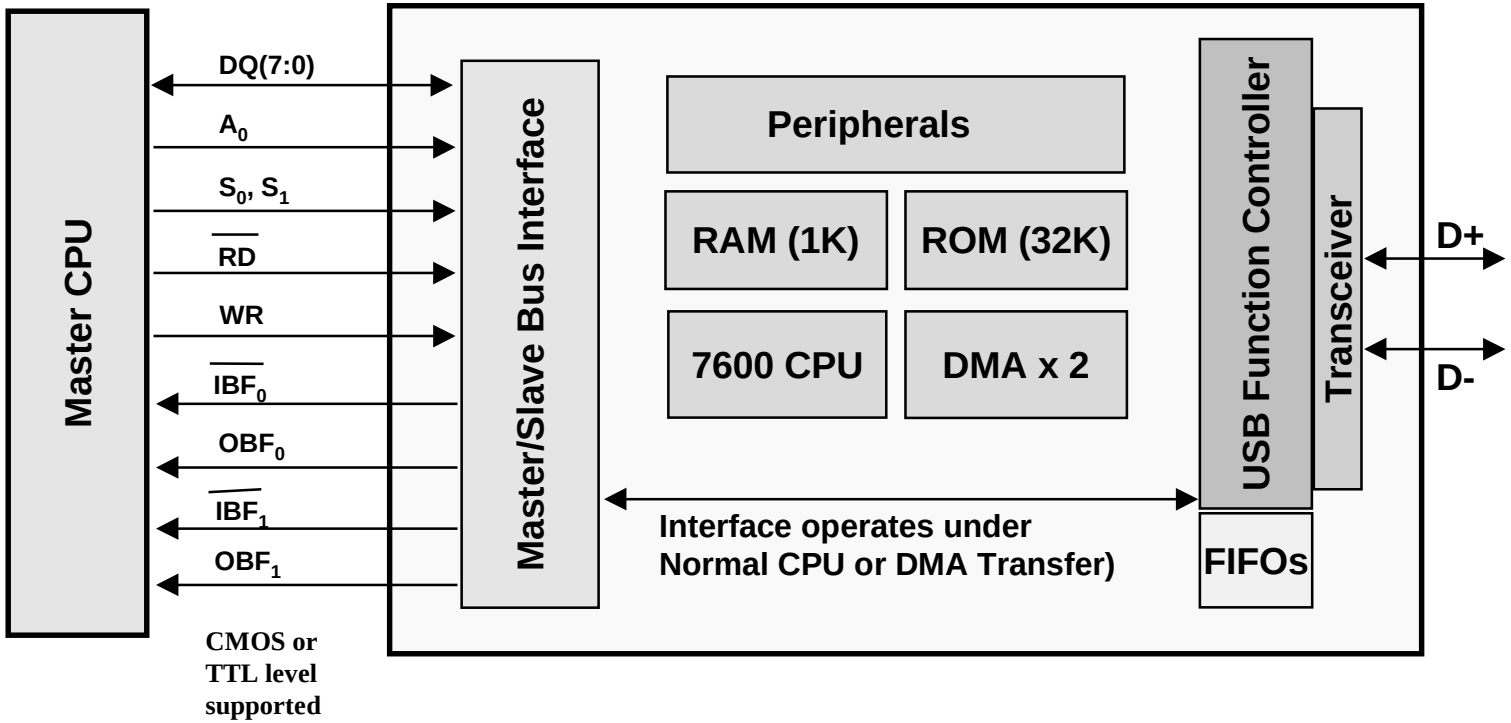
- Expanded Data Memory Access
  The Expanded Data Memory Access (EDMA) mode feature allows the user to access greater than 64 Kbyte data, via a banking scheme.

Two-Channel DMAC Main Features

- Two independent channels closely coupled with the USB and the Master CPU Bus Interface for efficient data transfers.
- Two cycles of F required per byte transferred. F = 12MHz
- Single-byte (4Mbs) and burst transfer (6Mbs) modes
- Transfer requests from USB (9), Master CPU Bus Interface (4), external interrupts (4), UART1 (2), UART2 (2), SIO (1), TimerX (1), TimerY (1), Timer1 (1), and software triggers
- 16-bit source and destination address registers (for a 64 Kbyte address space)
- 16-bit transfer count registers (for up to 64 Kbytes transferred before underflow)
- Source/Destination register automatic increment/decrement and no-change options
- Source/Destination/Transfer count register reload on write or after transfer count register underflow options.
- Fixed channel priority (Channel 0 > Channel 1)

Master CPU I/F with M37640: 8042 compatible

- The MBI enables communication with a Master 16-bit or 32-bit CPU at transfer rates up to ~3Mbytes; the Master is then free, while M37640 handles the local tasks.
- Minimal external interface/decoding logic required (depending on the system)



M37640 USB Function Controller Features V 1.1

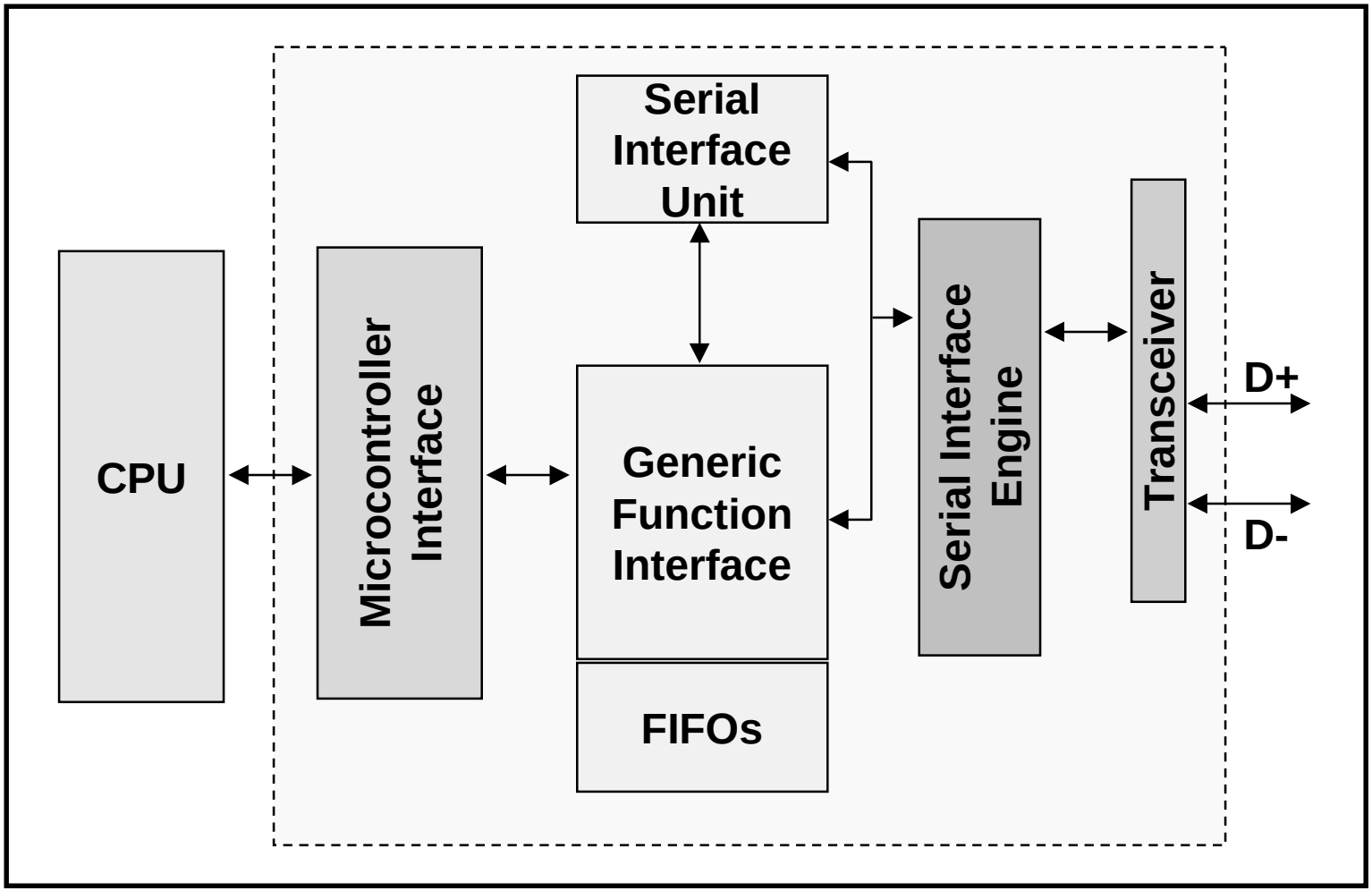
- Complete Device Configuration
- Supports all Device Commands
- Support of All USB Transfer Types:

  Isochronous, Bulk, Control, Interrupt
- Suspend/Resume Operation
- Self Powered Mode
- Error Handling capabilities

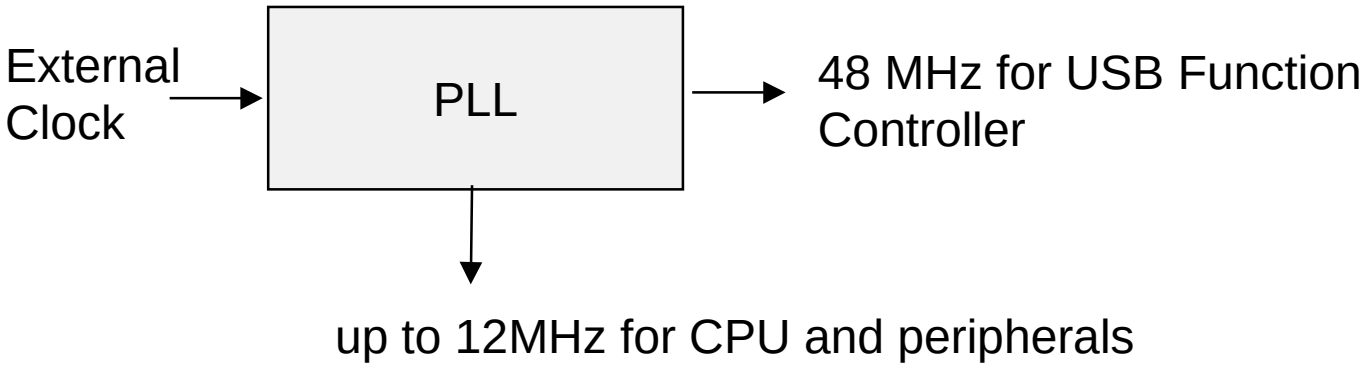
  CRC Errors, Data Retries, Response Time-Out, ID Error
- FIFOs

Endpoint 0:IN 16-byte	OUT 16-byte
Endpoint 1:IN 512-byte	OUT 800-byte
Endpoint 2:IN 32-byte	OUT 32-byte
Endpoint 3:IN 16-byte	OUT 16-byte
Endpoint 4:IN 16-byte	OUT 16-byte

USB Function Controller Block Diagram (M37640)



Frequency Multiplier



- 48MHz clock for USB eliminates the need for external clock oscillators
- On-chip clock generator minimizes EMI
- Generates MCU internal clock